

**MARKED-UP VERSION OF SPECIFICATION**

Semiconductor Integrated Circuit  
Having Transistor With Reduced Resistance

## BACKGROUND OF THE INVENTION

### 5 Technical Field

The present invention relates to a semiconductor integrated circuit, and particularly to a layout pattern for a semiconductor integrated circuit.

### Related Art

10 Conventionally, transistors utilizing high resistance polysilicon wiring have been used in MOS transistors that have to be protected against static electricity surges in the vicinity of pads of input protection circuits and output circuits, and surge voltage is relieved by utilizing resistive components of the polysilicon wiring.

15 Fig. 3 is a circuit diagram of an output circuit. Fig. 4-B is a layout pattern drawing of an NMOS transistor having conventional circuitry, and Fig. 4-A schematically shows a cross section of Fig. 4-B. The output circuit and the layout will now be described below using the drawings.

In the output circuit, the NMOS transistor 301 has a gate connected to an 20 output terminal 302 <sup>for receiving a signal</sup> from an internal circuit, a drain connected to an output terminal 303 and a source connected to GND 304. This NMOS transistor 301 is in a conducting state when a signal supplied to the gate is at an H level. At this time, an L level signal is output from the output terminal 303. When the signal supplied to the gate is an L level, the NMOS transistor 301 is in a non-conducting state, and at this time an H level signal is output from the output terminal 303.

The conventional pattern layout of an NMOS transistor used in this type of circuit will be described in more detail.

As shown in Fig. 4-A, the NMOS transistor has part of a source 405 30 connected to a polysilicon wiring layer 402 arranged ~~over~~ <sup>under</sup> a source region, via a first contact 401.

The polysilicon wiring layer 402 is connected to a first metal layer 403 arranged ~~on~~ <sup>over</sup> the same source 405 region, via a second contact 404. The first

<sup>1</sup>→ The layout pattern shown in Figs. 4-A and 4-B is disclosed in Japanese patent publication 6-232345, published on August 19, 1994.

metal layer 403 is connected to GND.

Part of the drain 406, similarly to part of the source 405, is connected to a conductor in the polysilicon wiring layer 402 arranged over the drain region, via the first contact 401. The polysilicon wiring layer 402 is connected to a first metal layer 403 arranged over the drain 406 region, via a second contact 404. The first metal layer 403 is connected to an output terminal.

Here, the contact 401 and the contact 404 are arranged so as to alternate, as shown in Fig. 4-B.

In the above described conventional circuit, the first contact 401 and the second contact 404 are alternately arranged without considering the difference between the resistance value of the first contact 401 and the resistance value of the second contact 404. Accordingly, the total resistance value of all the contacts will become large. There is thus a problem that the I-V characteristic of the MOS transistor will be degraded by this increase in the resistance value of the contact portions.

## SUMMARY OF THE INVENTION

An object of the present invention is to lower the overall resistance value. According to an example of the present invention, there is provided a semiconductor integrated circuit device, comprising, impurity diffusion regions formed as source and drain on a semiconductor substrate; a first conduction layer having a first resistivity formed over the impurity diffusion regions; a first contact hole group connecting the first conduction layer and the impurity diffusion regions; a second conduction layer having a second resistivity formed over the first conduction layer; and a second contact hole group connecting the first conduction layer and the second conduction layer at an upper part of the impurity diffusion region, and wherein the total number of contact holes is respectively different between the first contact hole group and the second contact hole group.

## BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a layout drawing showing a pattern layout of a first embodiment of the present invention.

Fig. 2 is an I-V characteristic drawing showing improved characteristics brought about by the present invention.

5 Fig. 3 is a circuit diagram of an output circuit.

~~FIGS. 4-A and 4-B are~~  
Fig. 4 is a layout drawing showing a pattern layout of the related art.

Fig. 5 is a circuit diagram of an input circuit.

~~FIGS. 6-A and 6-B are~~  
Fig. 6 is a layout drawing showing a pattern layout of a second embodiment of the present invention.

10

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

### (First Embodiment)

A circuit diagram showing an output circuit of a first embodiment of the 15 present invention is the same as Fig. 3. As shown in Fig. 3, the NMOS transistor 301 of the output circuit has a gate connected to an output terminal 302 from an internal circuit, a drain connected to an output terminal 303 and a source connected to GND 304. This NMOS transistor 301 is in a conducting state when a signal supplied to the gate is at an H level. At this time, an L level 20 signal is output from the output terminal 303. When the signal supplied to the gate is an L level, the NMOS transistor 301 is in a non-conducting state, and at this time an H level signal is output from the output terminal 303.

Fig. 1 is a drawing showing a pattern layout used in the case of the present invention. The layout structure of an NMOS transistor of the present 25 invention will now be described below using Fig. 1.

A polysilicon layer 102, constituting a first high resistance wiring layer, and a first metal layer 103, constituting a second low resistance wiring layer, are formed on respective regions of a source 105 and a drain 106.

Parts of the source 105 and drain 106 of the NMOS transistor are 30 connected to the first wiring layer, being the polysilicon layer 102, via a plurality of first contacts 101. The first contacts are each formed having a size of 0.6  $\mu\text{m}$  by 0.7  $\mu\text{m}$ . A contact resistance between the source or drain and the first wiring layer is 170  $\Omega/\text{unit}$  in terms of a sheet resistance.

The first wiring layer, being the polysilicon layer 102, and the second wiring layer, being a first metal layer 103, are connected via a plurality of second contacts 104. The first contacts are each formed having a size of 0.7  $\mu\text{m}$  by 0.7  $\mu\text{m}$ . A contact resistance between the first wiring layer 102 and the second wiring layer 103 is 9.5  $\Omega/\text{unit}$  in terms of sheet resistance.

Here, the contact resistance of portions of the source region 105 and the drain region 106 where the first contacts 101 are formed is larger than the contact resistance of portions where the second contacts 104 are formed.

As shown in Fig. 1, with respect to the pattern layout of the present invention, in order to lower the overall resistance, a plurality of first contacts 101 are arranged inside the area between the second contacts 104. In this embodiment, five first contacts 101 are arranged between two second contacts 104. An interval L1 between each first contact 101 is set to a fixed value of 1  $\mu\text{m}$ .

15 The distance L2 when a first contact 101 is adjacent to a second contact 104 is also a fixed value, and in Fig. 1 it is 1  $\mu\text{m}$ .

A distance L3 is a distance from the edge of the source 105 or drain 106 to a first contact hole 101, and distance L4 is a distance from a gate electrode to a first contact hole 101, and the first contact holes are arranged so that  $L_3 \geq L_4$ .

20 In this embodiment,  $L_3 = L_4 = 5.25 \mu\text{m}$ .  $L_3 = 5.25 \mu\text{m}$ .

The first metal layer 103 on the source region 105 is connected to GND, while the first metal layer 103 on the drain region 106 is connected to an output terminal.

The operation of the first embodiment of the present invention will be described below. The characteristic of drain current against drain voltage for the NMOS transistor (I-V characteristic) is shown in Fig. 2. The characteristic shown in Fig. 2 is a characteristic for the case where the ON resistance of the NMOS transistor 301 of Fig. 3 is 30.

If a layout pattern such as that in Fig. 1 is used, the resistance of the first contacts is 34  $\Omega$  (170/5) and the resistance of the second contacts is 4.8  $\Omega$  (9.5/2). Accordingly, the ON resistance of the NMOS transistor becomes  $30 + 34 + 4.8 = 68.8 \Omega$ . The drain voltage at which the NMOS transistor actually operates is approximately 1.6V. With the drain voltage at 1.6V in this case, a

current of 23.3 mA flows.

On the contrary, if the I-V characteristic is measured using the conventional pattern layout shown in Fig. 4-B, the resistance of the first contacts is  $56\Omega$  (170/3) and the resistance of the second contacts is  $2.4\Omega$  (9.5/4).

The overall ON resistance becomes  $30 + 56 + 2.4 = 88.4\Omega$ . In other words, with the drain voltage at 1.6V, a current of only 19 mA will flow.

With an I-V characteristic in a hypothetical ideal state where there is absolutely no contact resistance, a current of 52.8 mA will flow with a voltage of 1.6V. With the NMOS transistor using the pattern layout of the present invention, a current reduced to 44% compared to that of this ideal state will flow. Compared to this, a current flow in an NMOS transistor using the conventional pattern layout is reduced by more than 64%.

By using the present invention, an improvement of 20% can be expected.

In order to thus reduce the overall contact resistance, a plurality of first contacts 101 are arranged inside the area between the second contacts 104. As a result, compared to the related art, the overall contact resistance of the NMOS transistor is reduced, and the current driving capability is improved.

Since a plurality of first contacts 101 are arranged between the second contacts 104, overall, current will flow in either of the first wiring layer or the second wiring layer in a well balanced manner.

By setting the interval between the multiply arranged first contacts 101 to a predetermined fixed interval, the length of polysilicon wiring layer 101 between each contact 101 is equal. That is, the individual resistance of the polysilicon layer between the contacts 101 is equal. As a result, a surge voltage is uniformly distributed and overall protection against surge voltages is stable, even if a surge such as static is temporarily input to the output terminals.

The first contact holes are arranged so that a distance L3 from the edge of a source 105 or drain 106 to a first contact hole 101, and a distance L4 from a gate electrode to a first contact hole 101 satisfy  $L3 \geq L4$ . When surges such as static are input, the surge voltage will be converged on a portion located between an edge of the diffusion region and a first contact 101 extremely close to the edge, and there is no fear of damage to the diffusion region.

## (Second Embodiment)

Fig. 5 is a circuit diagram showing an input/output circuit of the second embodiment of the present invention. As shown in Fig. 5, an NMOS transistor 510 in the output circuit has a gate connected to an output terminal 503, from internal circuitry 502, a drain connected to an input/output terminal 501, and a source connected to GND 504. The NMOS transistor 510 is in a conducting state when an H level signal is supplied to the gate. At that time, an L level signal is output from the input/output terminal 501. When an L level signal is supplied to the gate, the NMOS transistor 510 is in a non-conducting state, and an H level signal is output to the input/output terminal 501.

The NMOS transistor 520 in the input circuit has a drain connected to the input/output terminal 501, and the source and gate are connected to GND 504. This NMOS transistor 520 functions as a protection element to shunt static surges etc., to the NMOS transistor 510 in the output circuit, and to the input/output terminal 501, to GND 504.

Fig. 6-A and Fig. 6-B respectively show pattern layouts for the NMOS transistor 510 and the NMOS transistor 520 in Fig. 5. The transistor layout structure of the present invention will be described below using Fig. 5 and Fig. 20-6-1 Figs. 6-A and 6-B.

As shown in Fig. 6-1 in the NMOS transistor 510 of the output circuit side in Fig. 5, a gate electrode 619 having a gate length  $LG$  of  $0.9 \mu\text{m}$  is formed over an active region of the NMOS transistor 510. A polysilicon layer 612 constituting a first high resistance wiring layer, and a first metal layer 613 constituting a second wiring layer, are formed on the active region of the source 615 and the drain 616.

The source 615 and drain 616 of the NMOS transistor are respectively connected to the polysilicon layer 612, being the first wiring layer, through a plurality of first contacts 611. The first contacts are formed having a size of  $0.6 \mu\text{m} \times 0.7 \mu\text{m}$ .

The polysilicon layer 612, being the first wiring layer, is connected to the first metal layer, being the second wiring layer, through a plurality of second contacts 614. The second contacts 614 are formed having a size of  $0.6 \mu\text{m} \times 0.7 \mu\text{m}$ .

0.7  $\mu\text{m}$ .

Here, the contact resistance of the source region 615, drain region 616 and the part where the first contacts 611 are formed, is larger than the contact resistance of the portion where the second contacts 614 are formed.

- 5 As shown in Fig. 6-A, with the pattern layout of the present invention, the first contacts 611 are multiply arranged at fixed intervals between the second contacts 614, so as to reduce the overall contact resistance. In this embodiment, the second contacts 614 are arranged at three places, and four first contacts are respectively arranged in portions positioned between neighboring contacts 614.
- 10 An interval L1 between adjacent first contacts has a fixed value of 1  $\mu\text{m}$ .

The contacts are arranged so that a distance L2 between an adjacent first contacts and second contact is always equal, and in this embodiment it is 1  $\mu\text{m}$ . A distance from the edge of the source region 615 or drain region 616 to a first contact 611 is termed L3, while a distance from a gate electrode to a contact is 15 termed L4, and the contacts are arranged to satisfy the relationship  $L3 \geq L4$ . In this embodiment  $L3 = L4 = 5.25 \mu\text{m}$ .  $L3 = 5.25 \mu\text{m}$ .

- In the input circuit side NMOS transistor 520 of Fig. 5, as shown in Fig. 6-B, a gate electrode 629 having a gate length  $LG$  of 0.9  $\mu\text{m}$  is formed over an active region 620 of the NMOS transistor 520. A polysilicon layer 622 20 constituting a first high resistance wiring layer, and a first metal layer 623 constituting a second wiring layer, are formed on the active region of the source 625 and the drain 626.

The relationship between the first and second contacts and the respective wiring layers is the same as the relationship in the output circuit. The input 25 circuit side differs from the output side only in that because the width of the active region is wider than the output circuit part, the number of second contacts is different from that on the output side, and second contacts are arranged at four places.

Specifically, an interval L1 between adjacent first contacts is the same as 30 an interval set in the transistor formed in the output circuit, and in this embodiment it is fixed at 1  $\mu\text{m}$ . An interval between first contacts and second contacts is also exactly the same as the interval set for the transistor formed in the output circuit, and that is also 1  $\mu\text{m}$  in this embodiment.

A detailed description will be given below of the operation when a static surge, as previously described, is applied to the input/output terminal 501 of Fig. 5.

When a negative voltage of -1000V, caused by static electricity etc., is applied to the <sup>input/output</sup> terminal 501 in Fig. 5, the NMOS transistors 510 and 520 are both in an ON state. The applied static electricity is shunted by the flow of current from GND to the input/output terminal 501.

When there is disparity between the input circuit side NMOS transistor 520 and the output circuit side NMOS transistor 510, the current for diverting the applied voltage will flow more in one transistor than the other. If more current flows in one transistor than the other, the load will be concentrated in the side having the increased current flow. Accordingly, protection of the overall circuit against static electricity etc. is lowered.

In the second embodiment, as has been described above, the gate lengths have been made equal in the input side and the output side. Contact arrangement intervals etc. have also been adjusted so as to be the same at the input side and the output side. With this type of structure, the same current flows in both of the NMOS transistors, and the load is evenly shared between the input side and the output side.

In the second embodiment, in addition to the effects of the first embodiment, the respective pattern layouts of the input side NMOS transistor and the output side NMOS transistor are constructed having the same relationship. In this way, it is possible to improve the resistance to static electricity etc. of the circuit overall.

The ratio of the number of first contacts to the number of second contacts in the invention described above is suitably variable according to the desired overall resistance etc., but in order to sufficiently obtain the effects of the present invention, the unit resistance of the first contacts is preferably designed so as to be no more than ten times the unit resistance of the second contacts.

30

~~CLAIMS.~~

## ABSTRACT

An increase in overall resistance value is prevented by having different contact resistances connecting between different wiring layers. A transistor has a first conductive layer having a first resistivity formed on an impurity diffusion regions, a first contact hole group connecting the first conductive layer and the impurity diffusion region, a second conductive layer having a second resistivity formed on the first conductive layer, and a second contact hole group connecting the first conductive layer and the second conductive layer at an upper part of the impurity diffusion region. The first contact hole group and the second contact hole group have a different total number of contact holes.